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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,912	06/24/2003	Bruce A. Rogers	GP-302680	2154

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EXAMINER

DOLE, TIMOTHY J

ART UNIT	PAPER NUMBER
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2858

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/602,912

Applicant(s)

ROGERS ET AL.

Examiner

Timothy J. Dole

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,4,6-8,10-13,15,18 and 20 is/are rejected.
- 7) ☒ Claim(s) 2,5,9,14,16,17 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 6, 7, 13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Crane.

Referring to claims 1 and 13, Crane discloses a diagnostic method and apparatus suitable for use in an automobile controller comprising: a power supply terminal (fig. 1 (output of volt source 12)) conducting a reference voltage (column 1, lines 54-58); a sampling circuit (fig. 1 (22) and (24) and column 1, lines 70-71) coupled to said power supply terminal and having an output terminal for providing sampled values of said reference voltage (column 1, lines 66-71); and a reference voltage diagnostic circuit (fig. 1 (20), (22), (24) and (30)) having an input terminal coupled to said output terminal of said sampling circuit (fig. 1), wherein said reference voltage diagnostic circuit maintains a historical value (fig. 1 (signal from voltage driver 30, to comparator circuits 22 and 24)) of said reference voltage over a predetermined time period, compares a current sampled value of said reference voltage (fig. 1 (signal from potentiometers 26 and 28, to comparator circuits 22 and 24)) to said historical value, and indicates a fault in said

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reference voltage in response to said current sampled value being different from said historical value by more than a predetermined threshold (column 1, lines 58-75).

Referring to claim 6, Crane discloses the apparatus as claimed, further comprising a power supply (fig. 1 (12)) for providing said reference voltage to said power supply terminal.

Referring to claim 7, Crane discloses the apparatus as claimed wherein said reference voltage diagnostic circuit indicates said fault in said reference voltage in response to either said current sampled value being greater than said historical value by more than a first predetermined threshold or by said current sampled value being less than said historical value by more than a second predetermined threshold (column 1, lines 58-73).

Referring to claim 15, Crane discloses the method as claimed, further comprising the step of calculating said historical value using said current value (column 1, lines 73-75).

3. Claims 8, 10-12, 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Bolz et al.

Referring to claims 8 and 18, Bolz et al. discloses a diagnostic method and apparatus suitable for use in an automobile controller comprising: first and second power supply terminals respectively conducting first and second reference voltages (U1) and (U2); a sampling circuit (R1 and R2) coupled to said first and second power supply terminals and having an output terminal for providing sampled values of said first and second reference voltages; and a reference voltage diagnostic circuit (ADC and K) having

an input terminal coupled to said output terminal of said sampling circuit, wherein said reference voltage diagnostic circuit compares a sampled value of said first reference voltage to a sampled value of said second reference voltage, and indicates a fault in at least one of said first and second reference voltages in response a difference between said sampled value of said first reference voltage and said sampled value of said second reference voltage being greater than a predetermined threshold (column 3, line 42 - column 4, line 3).

Referring to claim 10, Bolz et al. discloses the apparatus as claimed, wherein said reference voltage diagnostic circuit indicates said fault by storing a diagnostic error code in a memory location (column 3, line 66 – column 4, line 3).

Referring to claim 11, Bolz et al. discloses the apparatus as claimed, wherein said reference voltage diagnostic circuit comprises: a central processing unit (μ C) coupled to said output terminal of said sampling circuit; and a memory coupled to said central processing unit for storing an application program having a reference voltage diagnostic associated therewith which selectively indicates said fault in the first and second reference voltages (column 3, line 39 – column 4, line 3).

Referring to claim 12, Bolz et al. discloses the apparatus as claimed, further comprising first and second power supplies (UB) for providing said first and second reference voltages respectively to said first and second power supply terminals (column 3, lines 3-12).

Referring to claim 20, Bolz et al. discloses the method as claimed wherein said step of indicating comprises the steps of: determining a smaller one of said first and

second reference voltages (column 2, lines 22-28); and setting an error flag corresponding to said smaller one of said first and second reference voltages (column 3, line 66 – column 4, line 3).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crane in view of Bolz et al.

Referring to claim 3, Crane discloses the apparatus as claimed except wherein said reference voltage diagnostic circuit indicates said fault by storing a diagnostic error code in a memory location.

Bolz et al. discloses a voltage monitor wherein said reference voltage diagnostic circuit indicates said fault by storing a diagnostic error code in a memory location (column 3, line 66 – column 4, line 3).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the diagnostic error code of Bolz et al. into the apparatus of Crane for the purpose of determining faults and generating reset signals to protect the connected electronic components (column 3, line 66 – column 4, line 3).

Referring to claim 4, Crane discloses the apparatus as claimed except wherein said reference voltage diagnostic circuit comprises: a central processing unit coupled to said output terminal of said sampling circuit; and a memory coupled to said central processing unit for storing an application program having a reference voltage diagnostic, associated therewith which selectively indicates said fault in said reference voltage.

Bolz et al. discloses the apparatus as claimed, wherein said reference voltage diagnostic circuit comprises: a central processing unit (μ C) coupled to said output terminal of said sampling circuit; and a memory coupled to said central processing unit for storing an application program having a reference voltage diagnostic associated therewith which selectively indicates said fault in the first and second reference voltages (column 3, line 39 – column 4, line 3).

Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate the CPU and memory of Bolz et al. into the apparatus of Crane for the same purpose as given in claim 3, above.

Allowable Subject Matter

6. Claims 2, 5, 9, 14, 16, 17 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

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7. Applicant's arguments filed February 1, 2005 have been fully considered but they are not persuasive.

8. In response to Applicant's arguments with respect to claim 8, that Bolz et al. "does not disclose a sampling circuit having an output terminal for providing sampled values of first and second reference voltages" (page 8, lines 6-7), it should be noted that circuits R1 and R2 of Bolz et al. receive operating voltage UB and provide samples of it as reference voltages U1 and U2 (column, 3, lines 3-12).

9. In response to Applicant's arguments with respect to claim 8, that Bolz et al. "does not disclose a reference voltage diagnostic circuit that compares a sampled value of the first reference voltage to a sampled value of the second reference voltage" (page 8, lines 10-12), it should be noted that the ratio that Bolz et al. calculates is a comparison of the sampled first and second reference voltages (column 3, lines 39-49).

10. In response to Applicant's arguments with respect to claims 8 and 18, that Bolz et al. "does not disclose a reference diagnostic circuit that indicates a fault in response to a difference between the sampled values of two reference voltages" (page 8, lines 13-15 and 24-25), it should be noted that the ratio of Bolz et al. represents a difference between the reference voltages. If the reference voltages were the same, the ratio found by Bolz et al. would be 1. As the difference between the reference voltages increases the ratio will increase or decrease depending on which voltage is out of range. Therefore, when Bolz et al. compares the ratio with predetermined limits, the difference between the reference voltages is the parameter that is being monitored (column 3, lines 50-65).

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11. In response to Applicant's argument with respect to claim 10, that Bolz et al. "does not disclose the storing of a diagnostic error code in a memory location" (page 8, lines 18-19), it should be noted that the predetermined limit values must be stored in some sort of memory location, and there must be some sort of code to determine when the ratio leaves the range whereby setting the microcontroller to a safe state.

12. In response to Applicant's argument with respect to claim 20, that Bolz et al. "does not disclose the setting of an error flag corresponding to the smaller one of the two reference signals" (page 9, lines 1-2), it should be noted that if one of the voltages of Bolz et al. is out of range, a reset signal is activated (column 3, lines 13-19). Therefore, if the smaller reference voltage is out of range, an error flag will be set and the reset line will be activated.

13. Applicant's arguments with respect to claims 1 and 13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Dole whose telephone number is (571) 272-2229.

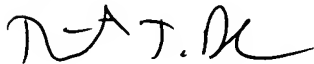
The examiner can normally be reached on Mon. thru Fri. from 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571) 272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJD



**ANJAN DEB
PRIMARY EXAMINER**